What is claimed is:

1. A method of forming semiconductor device, said method comprising the steps of:

providing a semiconductor substrate having a first conductive layer and an epi-layer doped with the same type impurities but is doped lightly than said first conductive layer;

forming a first oxide layer on said epi-layer;

performing a first ion implant through said first oxide layer to form a first region of a second conductive type buried in said epi-layer;

patterning said first oxide layer and recessing said epi-layer to form a plurality of trenches and forming a termination region at perimeter of said substrate;

recovering etching damage occurred during said patterning and driving impurities of said second conductive type;

forming a barrier metal layer on entire surfaces of said substrate;

performing a thermal anneal to form metal silicide layer by reacting material of said epi-layer with said barrier metal layer;

removing unreacted barrier metal layer;

forming a top metal layer on entire surfaces;

patterning said top metal layer to define an anode electrode;

removing layers formed on a backside surface of said semiconductor substrate during forgoing steps; and

forming a backside metal layer on said backside surface, said backside metal layer acted as a cathode.

2. The method according to Claim 1 and further comprising forming a first nitride layer on said first oxide layer thereafter said first nitride layer and said first oxide layer are patterned as a hard mask for trenches patterned formation.

3. The method according to Claim 1 wherein said step of patterning said first oxide layer and recessing said epi-layer comprising the step of :

forming a photoresist pattern on said fist oxide layer;

patterning said first oxide layer by wet etch;

recessing said epi-layer by using said patterned photoresist pattern as a mask; and removing said photoresist pattern.

4. The method according to Claim 1 wherein said step of recovering etching damage comprising the steps of:

performing a thermal oxidation to form a second oxide layer on sidewalls of said trenches by consuming said material of said epi-layer;

removing said second oxide layer by wet etch.

5. The method according to Claim 1 wherein said barrier metal layer is made of material selected from the group consisting of Ti, Ni, Cr, Mo, Pt, Zr, W and the combination thereof.

6. The method according to Claim 1 wherein said top metal layer is formed of the stacked layers of TiNi/Ag or TiW/Al.

7. A power rectifier device, comprising:

A semiconductor substrate having a first conductive layer doped with first-type impurities, an epi layer formed thereon which is extended

to a first surface thereof and is lightly doped with said first-type impurities;

a cathode metal layer formed on said first conductive layer opposite said first surface;

a first oxide layer formed on said first surface;

a pair of trenches formed into said epi-layer and spaced from each other by a first mesa region;

a termination mesa region surrounded said pair of cell trenches;

a second conductive type doped region formed into said epi layer of said first mesa region and said termination mesa region.

a Schottky barrier silicide layer formed on said epi layer in said trenches;

a top metal layer acted as an anode formed on said Schottky barrier silicide layer and extended to cover all surfaces of said first mesas region and a portion of said termination mesa region;

8. The power rectifier device according to Claim 7 and further comprising a nitride layer formed in between said first oxide layer and said top metal layer.

9. The power rectifier device according to Claim 8 wherein said first oxide layer has a thickness between about 100 - 1000 nm and said nitride layer has a thickness between about 50 - 300 nm

10. The power rectifier device according to Claim 8 wherein said trenches have a depth of between about 1 to 5μm measured from the surface of said epi layer.

11. The power rectifier device according to Claim 7 wherein said Schottky barrier silicide layer is formed of metal silicide selected from the group consisting of silicide of Ti, Ni, Cr, Mo, Pt, Zr, and W with silicon.

12. The power rectifier device according to Claim 7 wherein said top metal layer is formed of stacked layers of TiNi/Ag or TiW/Al.